REMARKS

The following remarks are provided in response to the Office Action dated August 18, 2004 in which the Examiner:

- objected to the drawings under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims;
- objected to claim 23 for reciting an element lacking an antecedent basis;
- rejected claims 1, 8, 19, 24, and 28 under 35 U.S.C. §102(b) as being anticipated by United States Patent No. 5,961,649 to Khandekar et al. (hereinafter Khandekar);
- rejected claims 2-6, 9, 11-18, and 21 under 35 U.S.C. §103(a) as being unpatentable over Khandekar in view of U.S. Patent No. 6,279,087 to Melo et al. (hereinafter Melo);
- rejected claims 10 and 30 under 35 U.S.C. §103(a) as being unpatentable over Khandekar in view of Heuring and Jordan, "Computer System Design and Architecture," (hereinafter Heuring);
- rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over Khandekar in view of U.S. Patent No. 6,064,247 to Krakirian; and
- rejected claims 20 and 22-23 under 35 U.S.C. §103(a) as being unpatentable over Khandekar in view of U.S. Patent No.6,631,484 to Born.

The applicants respectfully request reconsideration of the above referenced patent application in view of the amendments and remarks set forth herein, and respectfully request that the Examiner withdraw all rejections.

Drawing Objection

The Examiner objected to the drawings under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims. In particular, the Examiner alleges that the "asynchronous logic" per claim 7 and "deep memory node" per claims 19-23 must be shown in the drawings or that the feature(s) must be canceled from the claim(s). The applicants herein cancel claims 19-23.

The applicants assert that claim 7 is drawn to a method and that an appropriate illustration of a method is a flow chart as included in Figure 3. Element 315 of Figure 3 includes the label "creating a capture pulse with asynchronous logic." Accordingly, the applicants assert that "asynchronous logic" as recited by method claim 7 is properly shown in the drawings. Accordingly, the applicants affirm that they have overcome the Examiner's drawing objection.

Claim Objection

The applicants herein cancel claim 23.

35 U.S.C. §102(e)

The Examiner rejected claims 1, 8, 19, 24, and 28 under §102(b) as being anticipated by Khandekar. For at least the foregoing reasons the applicants traverse the Examiner's rejection.

To establish a *prima facie* case of anticipation under 35 U.S.C. §102, the Examiner must supply a single prior art document that alone teaches ". . . **every** aspect of the claimed invention either explicitly or impliedly." (emphasis added) (See M.P.E.P.

§706.02) If the Examiner cannot show that the single prior art document asserts each and every element and limitation of the applicants' claims, then the Examiner has failed to establish a *prima facie* case of anticipation for that claim. To overcome the Examiner's anticipation rejection, the applicants must only demonstrate that the cited prior art document fails to teach one element or limitation present in the claim.

Currently amended claim 1 recites in a salient portion:

> . . . creating a capture pulse **with asynchronous logic** to synchronize the media clock signal with a memory clock signal;
> (emphasis added)

Currently amended claim 24 recites a similar element. Claims 19-23 are herein canceled. With reference to dependent claims 7 and 27, an element of each incorporated into currently amended independent claims 1 and 24 respectively, the Examiner noted that "Khandekar does not discuss the details of how the capture pulse is produced," and further that "Khandekar does not disclose creating a capture pulse with asynchronous logic." The applicants agree. Accordingly, the applicants assert that currently amended claims 1 and 24 are patentable as each recites at least an element not taught by Khandekar. The applicants further assert that dependent claims 2-6, 8-10, 25-26, and 28-30 are patentable as each depends on a patentable independent claim.

35 U.S.C. §103(a)

The Examiner rejected claims 7 and 27 under §103(a) as being unpatentable over Khandekar in view of Krakirian. The applicant will respond with reference to currently amended independent claims 1 and 24 as they incorporate an element of dependent

claims 7 and 27 respectively. For at least the foregoing reasons the applicants traverse the Examiner's rejection.

A *prima facie* case of obviousness under 35 U.S.C. §103 requires, among other criteria, that ". . . the prior art reference (or references when combined) must teach or suggest **all** the claim limitations." (emphasis added) (See M.P.E.P. 706.02(j) and 2143.03). To overcome a §103(a) rejection, the applicants must only demonstrate that the cited prior art document or documents fail individually and in combination to teach or suggest one element or limitation present in the claim.

Currently amended claim 1 recites in a salient portion:

> . . . creating a capture pulse **with asynchronous logic** to synchronize the media clock signal with a memory clock signal;
> (emphasis added)

Currently amended independent claim 24 recites a similar element. The Examiner noted that Khandekar did not disclose creating a capture pulse with asynchronous logic. The applicants agree. The Examiner alleges, however, that Krakirian Figure 6A, Figure 8, and column 1 lines 54-61 teach asynchronous logic to generate a plurality of clock signals. The applicants respectfully disagree. The applicants point out that the Krakirian Abstract discloses generating multiple frequency clock signals using a single input clock signal. Further, "[t]he rising edges of all the clock signals generated are synchronized . . . ." (See Abstract, lines 6-8). Column 1, lines 54-57 recite that "[t]o allow synchronization of the operations performed by difference logic elements, typically one or more input clocks are provided which serve as **a reference clock signal for all logic elements in the integrated circuit**." (emphasis added). The applicants assert that all logic elements utilizing a singular reference clock signal cannot teach creating a capture pulse with

asynchronous logic as recited by currently amended independent claims 1 and 24. Accordingly, the applicants affirm that currently amended independent claims 1 and 24 are patentable over Khandekar in view of Krakirian. The applicants further submit that dependent claims 2-6, 8-10, 25-26, and 28-30 are patentable as each depends from a patentable independent claim.

The Examiner further rejected claims 2-6, 9, 11-18, and 21 under §103(a) as being unpatentable over Khandekar in view of Melo. For at least the foregoing reasons the applicants traverse the Examiner's rejection.

Currently amended independent claim 11 recites in a salient portion:

> . . . a synchronizer **including an asynchronous state machine**;
> (emphasis added)

The Examiner alleges that the Kandekar "transfer logic 38" element Figure 1, Figure 5, and column 3 lines 26-29 describe a synchronizer. In particular, the cited portions of the specification disclose that "[t]he transfer logic 3 further includes circuitry for synchronizing clock signals . . . ." The applicants assert, however, that the cited portions of Kandekar do not disclose a synchronizer including an asynchronous state machine as recited by currently amended independent claim 11. For example, Figures 3 and 5 illustrate circuits for transferring signals from one clock domain to another clock domain (e.g., fast to slow or slow to fast). The applicants affirm that there is neither indication of an asynchronous state machine in Figures 3 and 5 nor in the portions of the detailed description directed thereto. Accordingly, the applicants confirm that currently amended claim 11 is patentable as it recites at least an element not taught by Kandekar and Melo both individually and in combination. The applicants further assert that dependent claims 12-14 and 16-18 are patentable as each depends from patentable independent claim 11.

The applicants finally submit that dependent claims 2-6 and 9 are patentable as each depends from patentable independent claim 1 as demonstrated above and that claim 21 has been canceled.

The Examiner rejected claims 10 and 30 under §103(a) as being unpatentable over Khandekar in view of Heuring. The applicants reaffirm that dependent claims 10 and 30 are patentable as they depend from patentable independent claims 1 and 24 respectively as demonstrated above.

The Examiner rejected claims 20 and 22-23 under §103(a) as being unpatentable over Khandekar in view of Born. As noted, the applicants herein cancel claims 19-23.

CONCLUSION

For at least the foregoing reasons, the applicants submit that they have overcome the Examiner's rejections and that they have the right to claim the invention as set forth in the listed claims.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, L.L.P.

11/24/04
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